FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **BERG 99.01 CIP**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): **09/890471**

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US00/02543	**01 FEBRUARY 2000**	**02 FEBRUARY 1999**

TITLE OF INVENTION: **IMPROVED CIRCUIT BOARD MANUFACTURING PROCESS**

APPLICANT(S) FOR DO/EO/US: **BERG, N. Edward**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☒ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

Form PTO-2038 authorizing credit card payment.

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/890471	PCT/US00/02543	BERG 99.01 CIP

24. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$1000.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	**$860.00**
☒	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$710.00**
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$690.00**
☐	International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**
	ENTER APPROPRIATE BASIC FEE AMOUNT =	**$710.00**
	Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	40 - 20 =	20	x $18.00	**$360.00**
Independent claims	3 - 3 =	0	x $80.00	**$0.00**
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**
	TOTAL OF ABOVE CALCULATIONS =			**$1,070.00**
☒	Applicant claims small entity status. (See 37 CFR 1.27). The fees indicated above are reduced by 1/2.			**$535.00**
	SUBTOTAL =			**$535.00**
	Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +			**$0.00**
	TOTAL NATIONAL FEE =			**$535.00**
☐	Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			**$0.00**
	TOTAL FEES ENCLOSED =			**$535.00**
			Amount to be: refunded	$
			charged	$

a. ☐ A check in the amount of _____ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **08-1391** A duplicate copy of this sheet is enclosed.

d. ☒ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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24,315
REGISTRATION NUMBER

August 1, 2001
DATE

IN THE INTERNATIONAL BUREAU OF WIPO

APPLN. OF:	BERG	)
APPLN. NO:	PCT/US00/02543	)
FILED:	February 1, 2000	)
FOR:	Improved Circuit Board Manufacturing Process	)
DOCKET:	BERG 99.01 CIP PCT	)

International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

AMENDMENT OF CLAIMS UNDER ARTICLE 19

In response to the International Search Report mailed February 26, 2001, please replace claim pages 12-20 with the attached new claim pages.

The claims have been amended to address the objections under PCT Rule 66.2(a)(v). Additionally, claim 1 has been amended to clarify that the second circuit pattern on the bottom surface is different from the first circuit pattern on the top surface. This is nowhere disclosed nor suggested in U.S. Patent 3,795,047 which gratuitously suggests forming conductive strips on both sides of the dielectric material, without suggesting how to avoid short-circuits or cross-talk.

In the event there are any fee deficiencies or additional fees are payable, please charge them to our deposit account number 08-1391.

If there is a problem with this submission, or any further information is required, it is requested that the undersigned attorney be contacted by collect telephone call.

RESPECTFULLY SUBMITTED

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Attorney for Applicants
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CERTIFICATE OF EXPRESS MAILING

"Express Mail" Mailing Label No. EK913644940US

Date of Deposit March 13, 2001

I hereby certify that this paper and the papers listed thereon are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above, and is addressed to the International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

Signature of person mailing Kim Hood

Name of person mailing KIM GOOD

What is claimed is:

1. A method of forming a circuit board, comprising the steps of:

a. supplying a non-conducting substrate having a top surface and a bottom surface;

b. forming a plurality of conductive pathways between said top surface and said bottom surface;

c. forming a first circuit pattern on said top surface; and

d. forming a second different circuit pattern on said bottom surface.

2. The method of claim 1, further comprising the step of printing one or more circuit devices on said first circuit pattern and on said second circuit pattern.

3. The method of claim 2, wherein said circuit devices are selected from capacitors, inductors, resistors and transformers.

4. The method of claim 3, wherein said first circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of printing a solder mask on said non-solder component of said first circuit pattern and on said circuit devices printed on said first circuit pattern.

5. The method of claim 4, wherein said second circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of printing a solder mask on said non-solder component of said second circuit pattern and on said circuit devices printed on said second circuit pattern.

6. The method of claim 1, wherein said top surface comprises a first conductor and said bottom surface comprises a second conductor, and wherein step b further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas wherein each of said plurality of first exposed areas is disposed above one of said plurality of second exposed areas;

removing said first conductor from each of said plurality of first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said top surface and said bottom surface.

7. The method of claim 6, wherein the printing steps further comprise use of printing techniques selected from electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

8. The method of claim 7, wherein step c further comprises:

printing a plating resist mask on said top surface to define said first circuit pattern;

plating said top surface increase the thickness of said first circuit pattern;

removing said plating mask; and

removing said first conductor.

9. The method of claim 8, wherein said plating resist mask of step c is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

10. The method of step 9, wherein step d further comprises:

printing a plating resist mask on said bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing said second conductor.

11. The method of step 10, wherein said plating resist mask of step d is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

12. A method of forming a multilayer circuit board, comprising the steps of:

a. supplying a first substrate having a first top surface and a first bottom surface;

b. forming a plurality of electrically conductive pathways between said first top surface and said first bottom surface;

c. forming a first circuit pattern on said first top surface;

d. forming a second circuit pattern on said first bottom surface;

e. supplying a second substrate having a second top surface and a second bottom surface;

f. forming a plurality of electrically conductive pathways between said second top surface and said second bottom surface;

g. forming a third circuit pattern on said second top surface;

h. forming a fourth circuit pattern on said second bottom surface;

i. supplying a first insulating layer having a first side and a second side;

j. joining said first side of said first insulating layer to said first bottom surface, and joining said second side of said first insulating layer to said second top surface, such that said first insulating layer electrically insulates said second circuit pattern from said third circuit pattern;

k. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, and said fourth circuit pattern.

13. The method of claim 12, further comprising the step of printing one or more circuit devices on said first circuit pattern, on said second circuit pattern, on said third circuit pattern, and on said fourth circuit pattern.

14. The method of claim 13, wherein said circuit devices are selected from capacitors, inductors, resistors, and transformers.

15. The method of claim 12, wherein said first top surface comprises a first conductor and said first bottom surface comprises a second conductor, and wherein step b further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a

plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface;

16. The method of claim 15, wherein step c further comprises:

printing a plating resist mask on said first top surface to define said first circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said plating mask; and

removing said exposed first conductor.

17. The method of claim 16, wherein said plating resist mask of step c is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

18. The method of step 17, wherein step d further comprises:

printing a plating resist mask on said first bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing said second conductor.

19. The method of step 18, wherein said plating resist mask of step d is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

20. The method of claim 12, wherein said second top surface comprises a first conductor and said second bottom surface comprises a second conductor, and wherein step f further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of sad plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said second top surface and said second bottom surface;

21. The method of claim 20, wherein step g further comprises:

printing a plating resist mask on said second top surface to define said third circuit pattern;

plating said second top surface to increase the thickness of said third circuit pattern;

removing said plating mask; and

removing said first conductor.

22. The method of claim 21, wherein said plating resist mask of step g is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-

set mode.

23. The method of step 22, wherein step h further comprises:

printing a plating resist mask on said second bottom surface to define said fourth circuit pattern;

plating said second bottom surface to increase the thickness of said fourth circuit pattern;

removing said plating mask; and

removing said second conductor.

24. The method of step 23, wherein said plating resist mask of step h is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

25. The method of claim 12, further comprising the steps of:

l. supplying a third substrate having a third top surface and a third bottom surface;

m. forming a plurality of electrically conductive pathways between said third top surface and said third bottom surface;

n. forming a fifth circuit pattern on said third top surface;

o. forming a sixth circuit pattern on said third bottom surface;

p. supplying a second insulating layer having a first side and a second side;

q. joining said first side of said second insulating layer to said second bottom surface, and joining said second insulating layer to said third top surface, such that said second insulating layer electrically insulates said fourth circuit pattern from said firth circuit pattern; and

r. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, said fourth circuit pattern, said fifth circuit pattern, and said sixth circuit pattern.

26. The method of claim 25, wherein said third top surface comprises a first conductor and said third bottom surface comprises a second conductor, and wherein step m further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface.

27. The method of claim 26, wherein step n further comprises:

printing a plating resist mask on said first top surface to define said fifth circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said plating mask; and

removing said first conductor.

28. The method of claim 27, wherein said plating resist mask step n is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

29. The method of claim 28, wherein step o further comprises:

printing a plating resist mask on said first bottom surface to define said sixth circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing said second conductor.

30. The method of claim 29, wherein said plating resist mask of step o is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

31. A method of forming a circuit board, comprising steps in sequence of:

a. supplying a non-conducting substrate having a top surface and a bottom surface each covered with a top and a bottom metallic layer, respectively;

b. forming a pattern mask on the top and the bottom metallic layers, leaving exposed metallic patterns;

c. building up the exposed metallic patterns to increase the thickness thereof;

d. removing the pattern mask whereby to expose the metallic patterns; and

e. etching the metallic layer coated substrate from step d whereby to remove exposed metallic surfaces, while leaving intact at least a portion of the built-up metallic patterns.

32. The method of claim 31, wherein said pattern mask is applied by printing.

33. The method of claim 32, wherein said pattern mask is printed by electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

34. The method of claim 33, wherein said printing is effected employing a fusable ink.

35. The method of claim 34, wherein said fusible ink comprises a polymeric binder ink containing colloidal metal.

36. The method of claim 35, wherein the colloidal metal comprises colloidal silver or colloidal palladium.

37. The method of claim 32, including the step of pre-heating the substrate prior to printing.

38. The method of claim 37, where the board is preheated to a temperature in the range of 100°C-160°C.

39. The method of claim 31, wherein said exposed metallic patterns are built-up by plating.

40. The method of claim 12, and further comprising the step of removing the resulting structure from the first substrate.

IMPROVED CIRCUIT BOARD MANUFACTURING PROCESS

Field Of The Invention

The present invention relates to an improved process for forming a single-sided, double-sided, or a multilayer circuit board.

Background Of The Invention

Printed circuit (or wiring) boards are well known in the electronics field. In general, such boards consist of a dielectric resin impregnated substrate (e.g. of woven or non-woven glass fibers) that is adhered to a sheet or foil of conductive metal, generally copper, on at least one surface. Typical resins that can be used to impregnate the substrate include phenolic resins, epoxy resins, polyimides, polyesters and the like. The copper sheet or foil is joined to the semi-cured resin impregnated substrate using well known techniques, e.g. by application of heat and pressure.

Thereafter, electrical circuit patterns are formed on the copper layers by conventional techniques. For example, a layer of photoresist may be coated over the copper layer, exposed imagewise and developed to yield a relief resist image on the copper layer. The exposed copper is etched away and the resist image is removed, leaving the copper circuit pattern exposed. Elemental copper, like other pure metals, generally exhibits poor adhesion characteristics for bonding to dielectric resinous substrates typically used in circuit board manufacture, and intermediate conversion coatings are frequently helpful to enhance the adhesion of the metal to the substrate. Hence, the copper foil may be treated prior to being laminated to the resin substrate to form a layer of copper oxide, tin or other adhesion promoter on at least one surface. Various methods have been employed for this purpose. Examples of such methods are described in U.S. Pat. Nos. 2,955,974; 3,177,103; and 3,198,672, which are hereby incorporated by reference.

Printed circuit boards prepared as described above may be assembled to form multilayer printed circuit board constructions by stacking a predetermined number of boards one atop another. In such a construction, the cured or semi-cured polymeric non-conductive materials (such as epoxy resin impregnated fiberglass cloth) is in contact with the copper surface of the adjacent circuit board. The stacked circuit board

assembly may be laminated together by application of heat and pressure to form a multilayer printed circuit board.

Typical laminating conditions involve pressing the stacked boards between metallic plates at a pressure between about 200 psi to about 600 psi at a temperature of between about 150° C. to 205° C. for up to about 4 hours. The electrical circuit patterns on the outer layers may then be interconnected to the circuit patterns on the inner layers by drilling an array of holes through the multilayer assembly circuit boards. The through-holes in the assembled boards are then cleaned by treatment with dilute solutions of strong acids and the like. Thereafter, the through-holes may be plated with copper to render the sides of the holes conductive thereby completing the circuit between the outer layer and the inner layer circuit patterns.

Summary of the Invention

The present invention relates to improvements in circuit board manufacturing processes. In one aspect, the invention relates to imprinting techniques for manufacturing circuit boards. More particularly, in one aspect the invention relates to a method for making printed circuit boards utilizing printing techniques for direct contact masks that resist plating and metallic etching. Applicant's invention also includes methods for direct printing of conductors and circuit devices and insulators onto circuit boards. Masks that resist solder and electrical shields may also be printed on the circuits and the substrate. Component position and designations can be directly printed.

Various circuit devices can be directly printed onto circuit boards. These devices include capacitors, resistors, inductors, and transformers. For example, capacitors can be formed at desired locations by printing a conductor, then a dielectric, and then a second conductor to form a parallel plate capacitor. Conductors can cross each other by printing an insulating pattern on a conductor or conductors at the desired cross over point(s) and subsequently printing a crossing over conductor(s). The process will make multi-layers as well as two sided plated though hole types of printed circuit boards.

Printing on the metallic conductor for direct contact masks that resist plating and metallic etching can be done by:

a. Electro-photographic printer with chemically resistant toner.

b. Ink jet printer with chemically resistant ink.

c. Relief press printer with chemically resistant ink in either direct or off-set mode.

d. Lithographic press printer with chemically resistant ink in either direct or off-set mode

e. Intaglio press printer with chemically resistant ink in either direct or off-set mode.

f. By screen printing.

Use of these direct printing techniques results in better definition of etched circuitry than can be achieved using conventional processes. In addition, use of these direct printing techniques allows for manufacture of narrower conductors, giving higher circuit densities on a circuit board than could be achieved using conventional techniques.

Brief Description of the Drawings

The invention will be better understood from a reading of the following detailed description taken in conjunction with the drawings in which like reference designators are used to designate like elements, and in which:

FIG. 1 is a sectional view of a double-sided, metal clad, circuit board substrate;

FIG. 2 is a sectional view of the first and second steps in Applicant's circuit board manufacturing process showing a direct printed pattern mask;

FIG. 3 is a sectional view of the second step in Applicant's process;

FIG. 4 is a view similar to FIG. 3, of the next step in Applicant's process;

FIG. 5 is a sectional view of an intermediate step in Applicant's alternative process;

FIG. 6 is a top view of a first void formed in a first conductor disposed on the top surface of a circuit board substrate in accordance with Applicant's alternative process;

FIG. 7 is a bottom view of a second void formed in a second conductor disposed on the bottom surface of a circuit board substrate in accordance with Applicant's alternative process;

FIG. 8 is a sectional view of a via formed in a substrate;

FIG. 9 is a sectional view showing printing of a plating resist mask;

FIG. 10 is a sectional view showing plating of exposed portions of the top and bottom sides of a substrate;

FIG. 11 is a sectional view showing formation of a first circuit pattern and a second circuit pattern;

FIG. 12 is a sectional view of a plated via;

FIG. 13 is a sectional view showing direct printing of conductors onto a plated via;

FIG. 14 is a sectional view showing direct printing of circuit devices onto a substrate;

FIG. 15 is a sectional view showing the first step of a process to print crossing conductors onto a circuit board substrate;

FIG. 16 is a sectional view showing the second step of a process to print crossing conductors onto a circuit board substrate;

FIG. 17 is a top view showing printing of crossing conductors onto a circuit board substrate;

FIG. 18 is a sectional view showing printing of multiple crossing conductors onto a circuit board substrate;

FIG. 19 is a top view showing multiple crossing conductors printed onto a circuit board substrate;

FIG. 20 is a sectional view of printed shields disposed on printed circuit devices;

FIG. 21 is a sectional view showing printing of a solder mask onto a circuit board substrate;

FIG. 22 is a sectional view of a multilayer circuit board formed using Applicant's process;

FIG. 23 is a sectional view of a circuit board laminate formed using Applicant's process which includes a via connecting all layers of the laminate; and

FIG. 24 is a sectional view of a circuit board laminate formed using Applicant's process which includes a via connecting two of three component substrates.

Detailed Description Of The Preferred Embodiments

Turning to FIG. 1, the printed circuit board production process begins with non-

conducting substrate 10 which has top surface 12 and bottom surface 14. Substrate 10 can be formed from a fiber-reinforced thermoset composition, a molded thermoplastic material, a ceramic material, a glass material, a stiff cardboard material, and mixtures of same. Preferably, substrate 10 is a FR-4 type epoxy material. Substrate 10 is between about 0.008 and 0.124 inches thick, preferably between about 0.011 and about 0.062 inches thick.

First conductor 16 covers top surface 12 and second conductor 18 covers bottom surface 14. First conductor 16 and second conductor 18 are metallic films having a thickness between about 0.0002 and about 0.002 inches. First conductor 13 and second conductor 14 may be formed from the same or from different metals. First conductor 13 and second conductor are preferably both formed from copper.

Referring to FIG. 2, first pattern mask 20 is applied to portions of first conductor 16 leaving other portions of first conductor 16 exposed. For example, numeral 22 corresponds to an exposed area of first conductor 16. First pattern mask 20 may be applied by printing techniques, including electro-photographic (i.e. electrostatic) printing, ink jet printing, relief press printing or the like using either direct or off-set mode, and lithographic press printing or the like using either direct or off-set mode and screen printing. The inks used to form first pattern mask 20 are commercially available. Preferred inks include conventional size controlled laser printing inks which are applied and then heated to fuse the inks. If desired, the substrate may be pre-heated, e.g. to 100°C-160°C prior to printing.

Similarly, second pattern mask 24 is applied to portions of second conductor 18 leaving the remaining portions of second conductor 18 exposed. The same printing processes and inks are used as described above in conjunction with first pattern mask 20. Numeral 26 corresponds to such an exposed area of second conductor 18. Exposed areas 22 and 26 correspond to the location on substrate 10 where a conduction pathway, sometimes called a via, between top surface 12 and bottom surface 14 is desired. As those skilled in the art will appreciate, a plurality of vias may be required in any given circuit board.

The next step, FIG. 3, involves plating up the exposed areas at 30A, 32A using either electrochemical or electroless plating. The first and second pattern masks 20,24

are then removed, and the first and second conductor films 16,18 are etched back and removed completely except the underlying plated up areas which, due to their increased thickness, survive in part the etching step. See FIG. 4.

The process for forming a via is now illustrated. The portion of first conductor 16 in exposed area 22 is removed from top surface 12 to form void 30. At either the same time, or in a separate step, the portion of second conductor 18 in exposed area 26 is removed from bottom surface 14 to form void 32. The portion of first conductor 16 in exposed area 22, and the portion of second conductor 18 in exposed area 26, are preferably removed by chemical etching processes. Referring to FIG. 5, first pattern mask 20 and second pattern mask 24 are then removed. First pattern mask 20 and second pattern mask 24 may be removed in a single step, or in separate steps.

Referring to FIG. 6, void 30 is roughly cylindrical, with the walls of the cylinder being defined by first conductor 16 and the floor of the cylinder being defined by top surface 12. Referring to FIG. 6, void 32 is roughly cylindrical, with the walls of the cylinder being defined by second conductor 18 and the floor of the cylinder being defined by bottom surface 14. The diameters of void 30 and void 32 may be approximately equal, or they may be different.

Referring to FIGS. 7 and 8, via 34 is a hole drilled through substrate 10 connecting void 30 and void 32. Via 34 has a diameter equal to or smaller than the diameters of either void 30 and void 32. Via 34 may be formed using a laser device or by chemical means. Use of chemical means to place through-holes in a metal foil clad circuit board substrate is taught in U.S. Pat. No. 5,653,893, which is hereby incorporated herein. Alternately the substrate could be mechanically drilled without forming voids in the conductor surfaces 16 and 18 as described herein.

The vias formed and the remainder of the first and second conductors 16,18 are then plated, thereby providing conductive pathways between the top and bottom surfaces and build-up of metal on the exposed surfaces of conductors 16,18. Plating via wall 40 can be accomplished by using electro-less plating after applying a nucleating material such as colloidal palladium or palladium sulfite and powdered silver. In this plating step, the remaining portions of first conductor 16 and 18 are

also plated. Alternatively, electroplating of the holes can be effected before or after the circuit pattern masks are applied as described below, by seeding the holes with a conductive ink comprised of polymeric binders with powdered graphite and powdered silver which is squeegied into the holes, excess ink drawn out, e.g. by means of a vacuum, and the substrate baked.

Referring to FIG. 9, pattern masks for plating resist are then printed on certain portions of conductors 36 and 38. These pattern masks are "negatives" of the desired circuits, and do not cover the vias already formed. For example, masks 42 and 44 are printed on conductor 36, and masks 46 and 48 are printed on conductor 38. As before, these masks can be printed using electro-photographic printing (electrostatic) using conventional size controlled laser printing inks or the like, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode or screen printing.

The exposed portions of conductors 36 and 38 comprise the desired circuit pattern. These exposed portions and the already-formed vias are again plated by electro or electroless means to enhance the thickness of the desired conduction pathways. Referring to FIG. 10, conductors 50, 52, 54, and 58 are plated to give a thickness of between about 0.0005 and about 0.001 inches. In addition, via wall 56 is plated to give a thickness of between about 0.0005 and about 0.001 inches.

Referring to FIG. 11, the plating masks are removed and entire substrate is etched, removing the electro-less(or metallization) plating which the circuit masks covered and the thin beginning conducting layer leaving only the desired conducting circuits and plated vias. Circuit elements, shields, and screens can then be printed.

In a separate embodiment, conductors and circuit components can also be formed by the printing processes described previously. Referring to FIG. 12, substrate 68 has been processed in the manner described in FIGs. 1-11. Substrate 68 includes conductor 70, conductor 72, via 74, and plated via wall 76, all of which are formed in the manner described above. Referring to FIG. 13, conductors 80, 82, and 84 are formed by direct printing methods using electrically-conductive inks. The inks used to form these conductors preferably comprise 80-90 percent polymeric binders, with the balance comprising powdered graphite and colloidal silver. Preferred inks comprise inks with a

high wax content.

Circuit elements can be printed in a desired array between desired conductor points. Referring to FIG. 14, component 86 is printed onto substrate 68 so as to connect to conductor 70 and conductor 82. Similarly, component 88 is printed onto substrate 68 so as to connect to conductor 72 and conductor 84.

For example, capacitors can be made by printing conductive plates where capacitors are desired. Over these plates is printed a dielectric. Over the dielectric is printed the top conductive plate and connection. A resistor can be formed by printing one or more layers between two conductors using a resistive ink. An inductor can be formed by printing one or more layers between two conductors using an ink having a magnetic permeability.

Referring to FIG. 13, conductors that cross over other conductors are made by first making bottom conductors in the methods previously described. For example, conductors 70, 72, 80, 82, and 84 are formed as described above. Referring to FIG. 15, insulator 90 is printed by the methods describer herein, over conductor 80 in the location where a crossover conductor is desired. The insulator may be printed over the entire surface except where conductors between insulating layers (vias) are desired. Similarly, insulator 92 is printed over conductor 84 in the location where a crossover conductor is desired. Referring to FIG. 16, crossing conductor 94 is then printed, by the methods described herein, crossing over conductor 80 where conductor 80 is covered by insulator 90. Similarly, crossing conductor 96 is printed so as to cross over conductor 84 where conductor 84 is covered by insulator 92. FIG. 17 shows a top view of substrate 68, conductors 70, 80, and 84, as well as insulators 90 and 92 and crossing conductors 94 and 96. Printing may be done in selective areas as illustrated or by printing a multiplicity of conductors and insulators or a layer of conductors and insulators.

Multiple layers of crossing conductors can be formed by printing insulators over any previous crossing conductor layer where a second crossover is desired. Referring to FIG.s 18 and 19, conductor 84, first insulator 92, and first crossing conductor 96 are formed as described above. Second insulator 100 is then printed over first crossing conductor 96. Second crossing conductor 102 is then printed over second insulator 100 to form multiple layers of crossing conductors. Such multilayer conductors can be used,

for example, to print a transformer device onto a circuit board where primary windings and secondary windings are printed over one or more layers of a printed material having a magnetic permeability.

Shields can then be printed over the appropriate conductors and circuit elements utilizing the desired printing techniques with appropriate inks. Referring to FIG. 20, conductors 112 and 114 are formed on substrate 110 using the methods described above. Shield 116 is then printed, using the printing techniques described herein, over conductor 112, and shield 118 is printed over conductor 114. In addition, solder masks can be printed on areas where solder adhesion is not desired. Soldering is normally done to connect circuit elements to the printed circuit board. As those skilled in the art will appreciate, such soldering is preferably done using automated wave soldering equipment. Referring to FIG. 21, solder masks 122, 124, and 126 are printed over certain portions of substrate 120 so that solder will not adhere to those portions when substrate 120 is passed through a wave soldering device. The printing techniques may be used to print directly on a screen or on an offset intermediary which could be used to transfer the image to the screen which could be used in screening on the solder mask.

Multi-layered structures are made by interleaving individual substrates with their layers of conductors, insulators and components, and insulating layers, where each of the individual substrates is first formed as previously described. After bonding the multiple substrates and insulating layers to form a laminate, the top and bottom surfaces of that laminate are processed like a "thick" beginning substrate. Referring to FIG. 22, laminate 130 is formed from substrates 132, 134, and 136, and insulating layers 138 and 140. Insulating layer 138 electrically insulates bottom surface 142 of substrate 132 from top surface 144 of substrate 134. Similarly, insulating layer 140 electrically insulates bottom surface 146 of substrate 134 from top surface 148 of substrate 136. Alternatively, these insulating layers may be formed direct by printing techniques described herein.

Top surface 144 and bottom surface 146 of substrate 134 are processed in the manner described using direct printing techniques above prior to lamination. Bottom surface 142 of substrate 132, and top surface 148 of substrate 136, are processed using the direct printing techniques described above prior to formation of laminate 130.

Insulating layers 138 and 140 may comprise an adhesive material or a separate

adhesive material may be used to join substrates 132, 134, and 136 with insulating layers 138 and 140 to form laminate 130. Adhesives used include epoxy resins, cyanoacrylate monomers and oligomers, polyurethanes, and mixtures thereof. The top surface 140 and bottom surface 150 are left blank until after the bonding process after which they processed using the direct printing methods described above.

Holes for interlayer connections are made in each substrate. These holes make the desired connections to the appropriate inner layer(s). Holes for though hole components are made "oversized" in each separate substrate and final drilled after the bonding process. The through component holes are made "oversized" since they will be multiply plated when the top and bottom surfaces of the bonded substrates are processed. This will reduce the hole size to the desired size.

Referring to FIG. 23, laminate 160 is formed in the manner described above from substrates 162, 164, and 166. After joining those substrates to form laminate 160, via 168 is formed as described above and via wall 170 is plated. This plated via electrically connects conductor 190 disposed in surface 172, conductor 192 disposed in surface 174, conductor 194 disposed in surface 176, conductor 196 disposed in surface 178, and conductor 198 disposed in bottom surface 182.

In an alternative embodiment, laminate substrates can be formed in a series of steps so as to allow electrical interconnection of only certain layers. Referring to FIG. 24, laminate 200 is formed from substrates 202, 206, and 210, and interleaved insulating layers 204 and 208. However, a sublaminate is first formed from insulating layer 208 and substrates 206 and 210. Via 248 having plated wall 250 is then formed through that sublaminate. Insulating layer 204 and substrate 202 are then joined to the sublaminate.

Plated via wall 250 electrically connects conductors 230 and 232 disposed on surface 216, conductors 234 and 236 disposed on surface 218, conductors 238 and 240 disposed on surface 220, and conductor 242 disposed on bottom surface 222. However, plated via wall 250 does not electrically connect to any conductors disposed on surfaces 212 or 214 of substrate 202 because insulator 204 insulates plated via wall 250 from substrate 202. Via 244 having plated via wall 246 electrically connects conductor 224 disposed on top surface 212 to conductors 226 and 228 disposed on surface 214.

Still other changes are possible. For example, through holes may be mechanically drilled, in which case the masking, etching and plating steps for hole formation may be eliminated. Also, in another embodiment of the invention, a multi-layer board may be built up by printing layers of conductors, insulators, circuit elements, etc. as above described, and the resulting multi-layer board stripped from the beginning substrate which then may be discarded or reused. In yet another embodiment, the image could be printed from the appropriate inks utilizing a silk screen or the like, and "screen printed" on the substrate.

What is claimed is:

1. A method of forming a circuit board, comprising the steps of:

a. supplying a non-conducting substrate having a top surface and a bottom surface;

b. forming a plurality of conductive pathways between said top surface and said bottom surface;

c. forming a first circuit pattern on said top surface; and

d. forming a second circuit pattern on said bottom surface.

2. The method of claim 1, further comprising the step of printing one or more circuit devices on said first circuit pattern and on said second circuit pattern.

3. The method of claim 2, wherein said circuit devices are selected from the group consisting of capacitors, inductors, resistors, transformers, and mixtures thereof.

4. The method of claim 3, wherein said first circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of printing a solder mask on said non-solder component of said first circuit pattern and on said circuit devices printed on said first circuit pattern.

5. The method of claim 4, wherein said second circuit pattern comprises a solderable component and a non-solder component, and further comprising the step of printing a solder mask on said non-solder component of said second circuit pattern and on said circuit devices printed on said second circuit pattern.

6. The method of claim 1, wherein said top surface comprises a first conductor and said bottom surface comprises a second conductor, and wherein step b further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas is disposed above one of said plurality of second exposed areas;

removing said first conductor from each of said plurality of first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said top surface and said bottom surface.

7. The method of claim 6, wherein the printing steps further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer

8. The method of claim 7, wherein step c further comprises:

printing a plating resist mask on said top surface to define said first circuit pattern;

plating said top surface increase the thickness of said first circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

9. The method of claim 8, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

10. The method of step 9, wherein step d further comprises:

printing a plating resist mask on said bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

11. The method of step 10, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic

printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

12. A method of forming a multilayer circuit board, comprising the steps of:

a. supplying a first substrate having a first top surface and a first bottom surface;

b. forming a plurality of electrically conductive pathways between said first top surface and said first bottom surface;

c. forming a first circuit pattern on said first top surface;

d. forming a second circuit pattern on said first bottom surface;

e. supplying a second substrate having a second top surface and a second bottom surface;

f. forming a plurality of electrically conductive pathways between said second top surface and said second bottom surface;

g. forming a third circuit pattern on said second top surface;

h. forming a fourth circuit pattern on said second bottom surface;

i. supplying a first insulating layer having a first side and a second side;

j. joining said first side of said first insulating layer to said first bottom surface, and joining said second side of said first insulating layer to said second top surface, such that said first insulating layer electrically insulates said second circuit pattern from said third circuit pattern;

k. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, and said fourth circuit pattern.

13. The method of claim 12, further comprising the step of printing one or more circuit devices on said first circuit pattern, on said second circuit pattern, on said third circuit pattern, and on said fourth circuit pattern.

14. The method of claim 13, wherein said circuit devices are selected from the group consisting of capacitors, inductors, resistors, transformers, and mixtures thereof.

15. The method of claim 12, wherein said first top surface comprises a first conductor and said first bottom surface comprises a second conductor, and wherein step b further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface.

16. The method of claim 15, wherein step c further comprises:

printing a plating resist mask on said first top surface to define said first circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

17. The method of claim 16, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

18. The method of step 17, wherein step d further comprises:

printing a plating resist mask on said first bottom surface to define said second circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

19. The method of step 18, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

20. The method of claim 12, wherein said second top surface comprises a first conductor and said second bottom surface comprises a second conductor, and wherein step f further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said second top surface and said second bottom surface.

21. The method of claim 20, wherein step g further comprises:

printing a plating resist mask on said second top surface to define said third circuit pattern;

plating said second top surface to increase the thickness of said third circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

22. The method of claim 21, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

23. The method of step 22, wherein step h further comprises:

printing a plating resist mask on said second bottom surface to define said fourth circuit pattern;

plating said second bottom surface to increase the thickness of said fourth circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

24. The method of step 23, wherein the printing step further comprises use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

25. The method of claim 12, further comprising the steps of:

l. supplying a third substrate having a third top surface and a third bottom surface;

m. forming a plurality of electrically conductive pathways between said third top surface and said third bottom surface;

n. forming a fifth circuit pattern on said third top surface;

o. forming a sixth circuit pattern on said third bottom surface;

p. supplying a second insulating layer having a first side and a second side;

q. joining said first side of said second insulating layer to said second bottom surface, and joining said second side of said second insulating layer to said third top surface, such that said second insulating layer electrically insulates said fourth circuit pattern from said fifth circuit pattern; and

r. forming a plurality of electrically conductive pathways between said first circuit pattern, said second circuit pattern, said third circuit pattern, said fourth circuit pattern, said fifth circuit pattern, and said sixth circuit pattern.

26. The method of claim 25, wherein said third top surface comprises a first conductor and said third bottom surface comprises a second conductor, and wherein step m further comprises the steps of:

printing an etch resist mask over a portion of said first conductor to form a plurality of first exposed areas;

printing an etch resist mask over a portion of said second conductor to form a plurality of second exposed areas, wherein each of said plurality of first exposed areas on said top surface is disposed above one of said plurality of second exposed areas on said bottom surface;

removing said first conductor from each of said first exposed areas to form a plurality of first void areas on said top surface;

removing said second conductor from each of said plurality of second exposed areas to form a plurality of second void areas on said bottom surface;

forming a plurality of vias by connecting one of said plurality of first void areas with one of said plurality of second void areas;

plating said plurality of vias to form said plurality of conductive pathways between said first top surface and said first bottom surface.

27. The method of claim 26, wherein step n further comprises:

printing a plating resist mask on said first top surface to define said fifth circuit pattern;

plating said first top surface to increase the thickness of said first circuit pattern;

removing said plating mask; and

removing any exposed first conductor.

28. The method of claim 27, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, and lithographic press printing using either direct or off-set mode.

29. The method of claim 28, wherein step o further comprises:

printing a plating resist mask on said first bottom surface to define said sixth circuit pattern;

plating said bottom surface to increase the thickness of said second circuit pattern;

removing said plating mask; and

removing any exposed second conductor.

30. The method of claim 29, wherein the printing step further comprise use of printing techniques selected from the group consisting of electro-photographic printing, ink jet printing, relief press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

31. A method of forming a circuit board, comprising the steps in sequence of:

a. supplying a non-conducting substrate having a top surface and a bottom surface each covered with a top and a bottom metallic layer, respectively;

b. forming a pattern mask on the top and the bottom metallic layers, leaving exposed metallic patterns;

c. building-up the exposed metallic patterns to increase the thickness thereof;

d. removing the pattern mask whereby to expose the metallic patterns; and

e. etching the metallic layer coated substrate from step d whereby to remove exposed metallic surfaces, while leaving intact at least a portion of the built-up metallic patterns.

32. The method of claim 31, wherein said pattern mask is applied by printing.

33. The method of claim 32, wherein said printing comprises electro-photographic printing, ink jet printing, release press printing using either direct or off-set mode, lithographic press printing using either direct or off-set mode, and screen image transfer.

34. The method of claim 33, wherein said printing is effected employing a fusable ink.

35. The method of claim 34, wherein said fusble ink comprises a polymeric binder ink containing colloidal metal.

36. The method of claim 35, wherein the colloidal metal comprises colloidal silver or colloidal palladium.

37. The method of claim 32, including the step of pre-heating the substrate prior to printing.

38. The method of claim 37, where the board is preheated to a temperature in the range of 100°C-160°C.

39. The method of claim 31, wherein said exposed metallic patterns are built-up by plating.

40. The method of claim 12, and further comprising the step of removing the resulting multiplayer circuit board from the first substrate.

Abstract

An improved method for manufacturing circuit boards which utilizes direct printing methods to form conductor patterns from metal foils disposed on one or both sides of a conventional substrate, to form conductors directly onto a circuit board substrate, to form circuit devices directly onto a circuit board substrate, to form shields directly on circuit patterns, to form solder masks directly on circuit patterns, and to form multilayer circuit board laminates. The circuit devices formed using Applicant's direct printing processes include capacitors, resistors, inductors, and transformers.

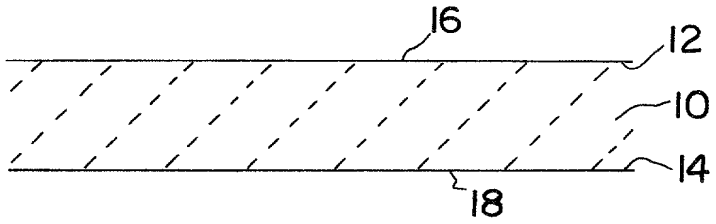

FIG. 1

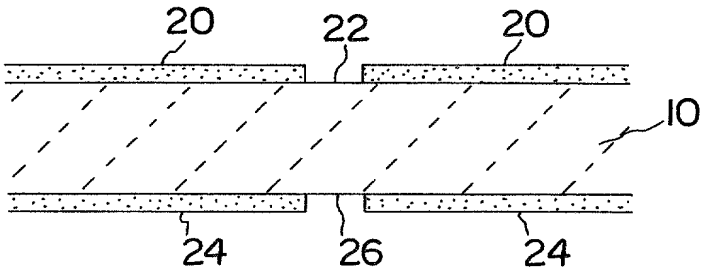

FIG. 2

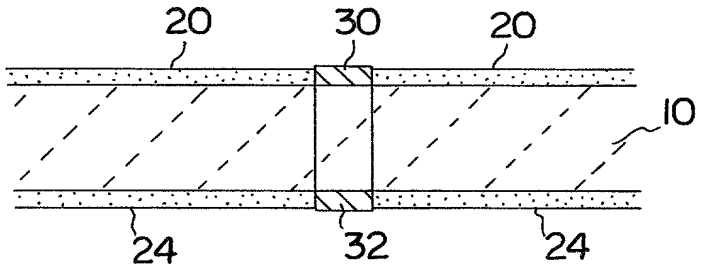

FIG. 3

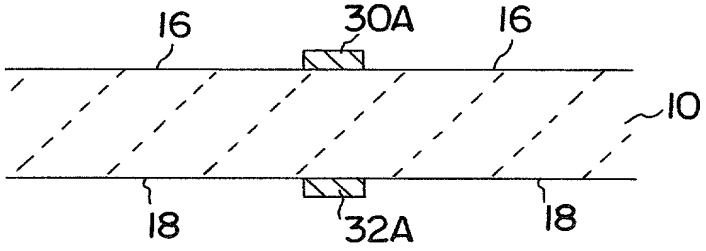

FIG. 4

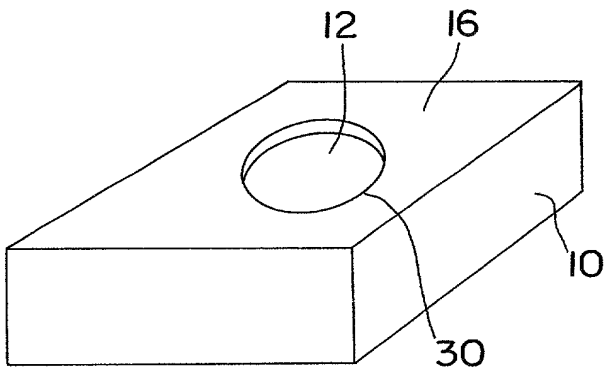

FIG. 5

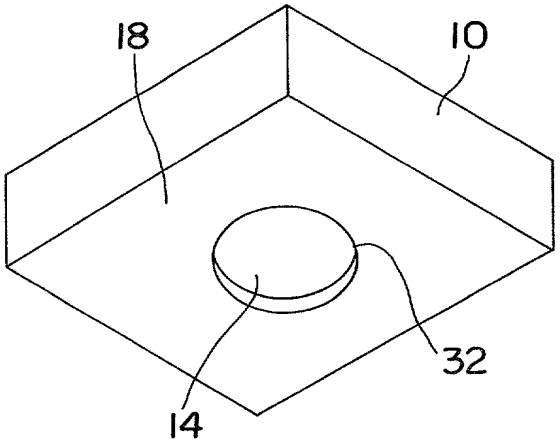

FIG. 6

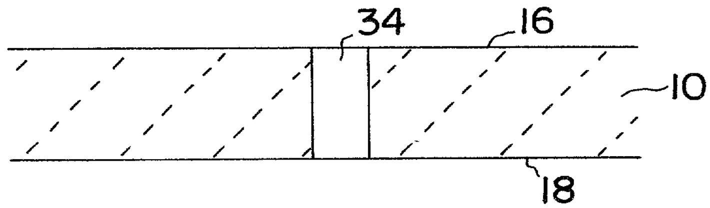

FIG. 7

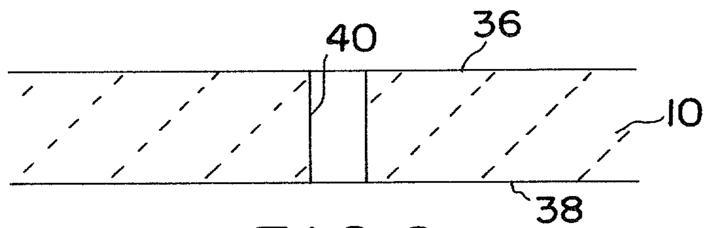

FIG. 8

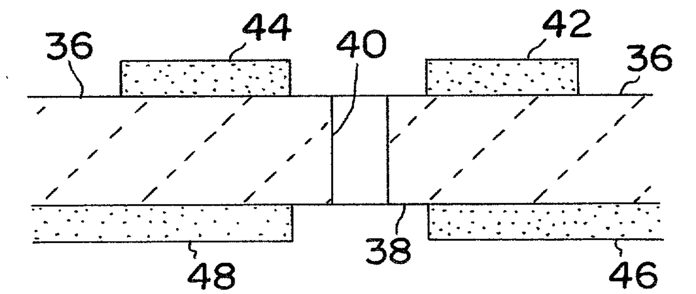

FIG. 9

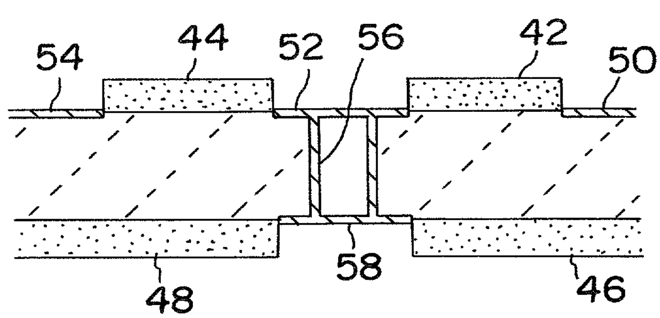

FIG. 10

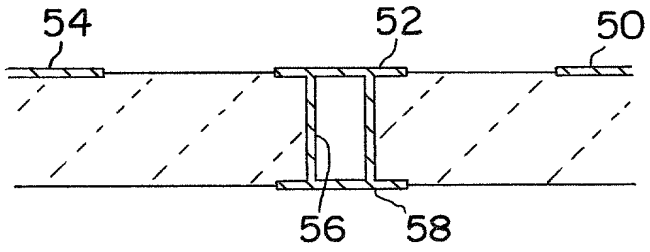

FIG. 11

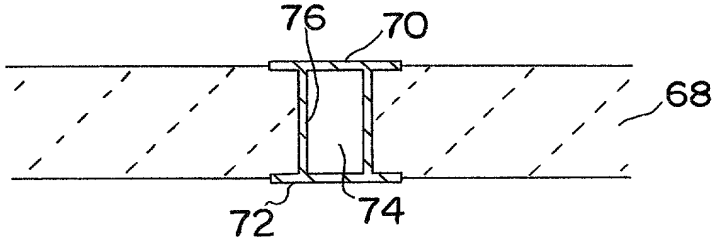

FIG. 12

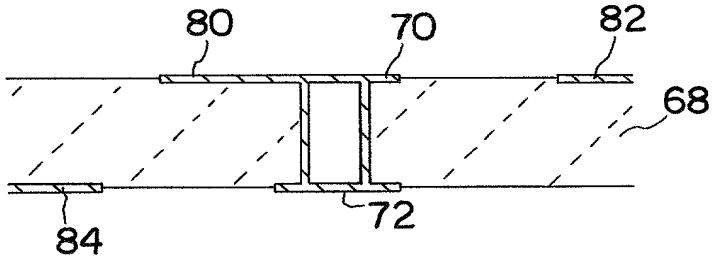

FIG. 13

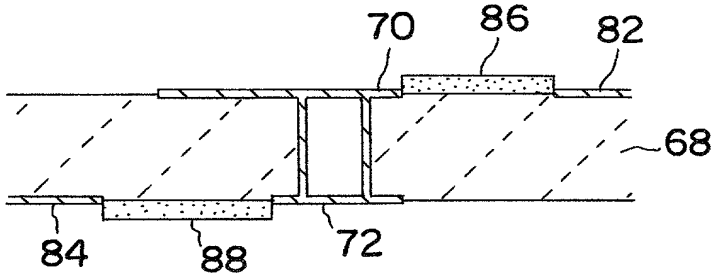

FIG. 14

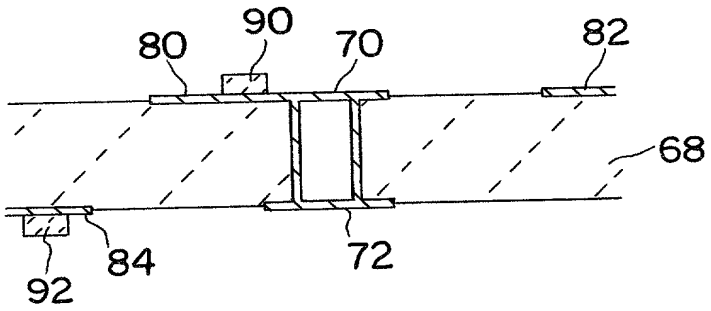

FIG. 15

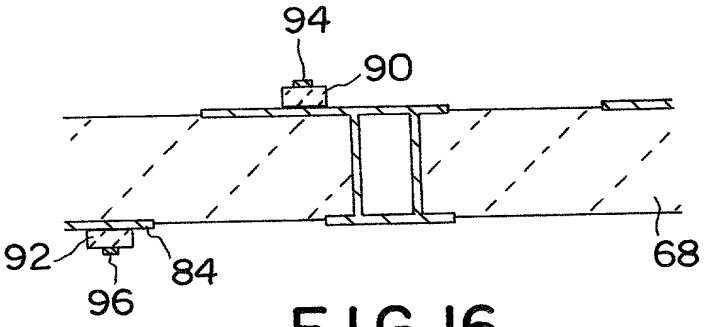

FIG. 16

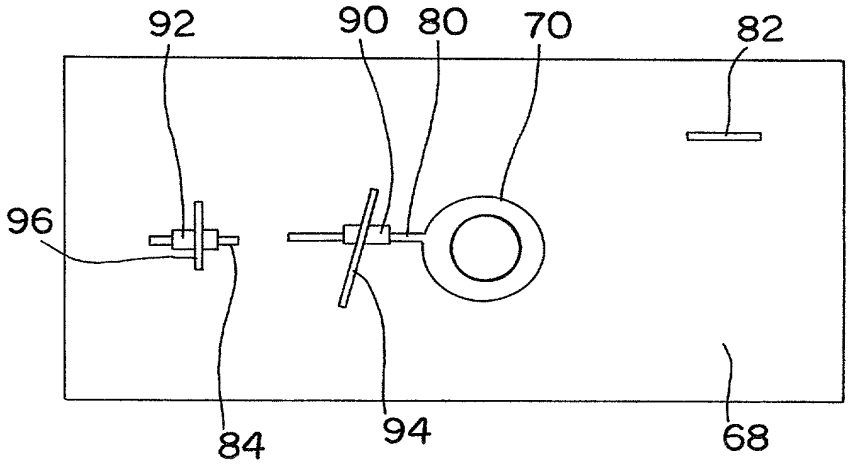

FIG. 17

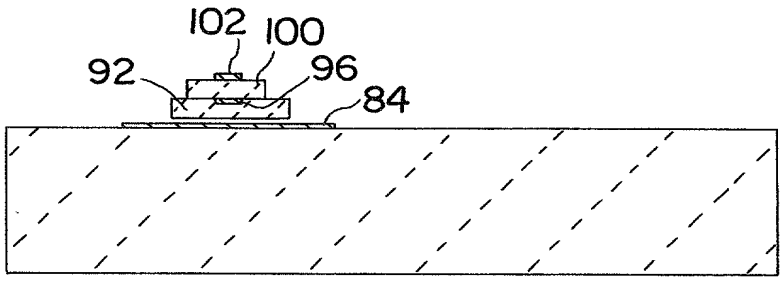

FIG. 18

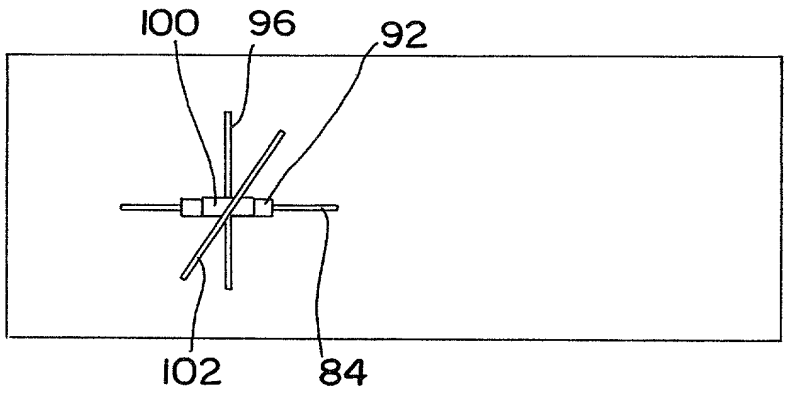

FIG. 19

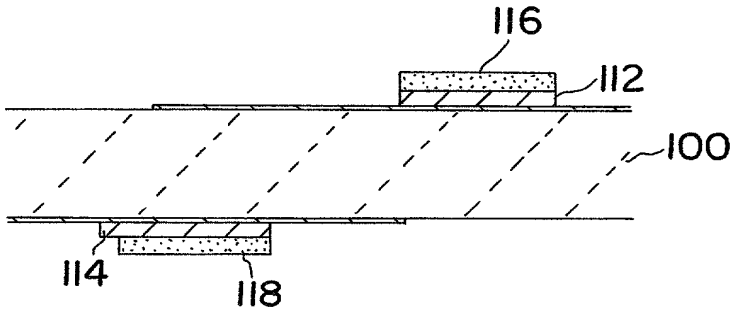

FIG. 20

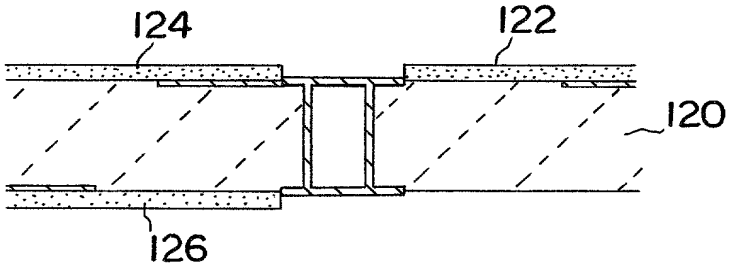

FIG. 21

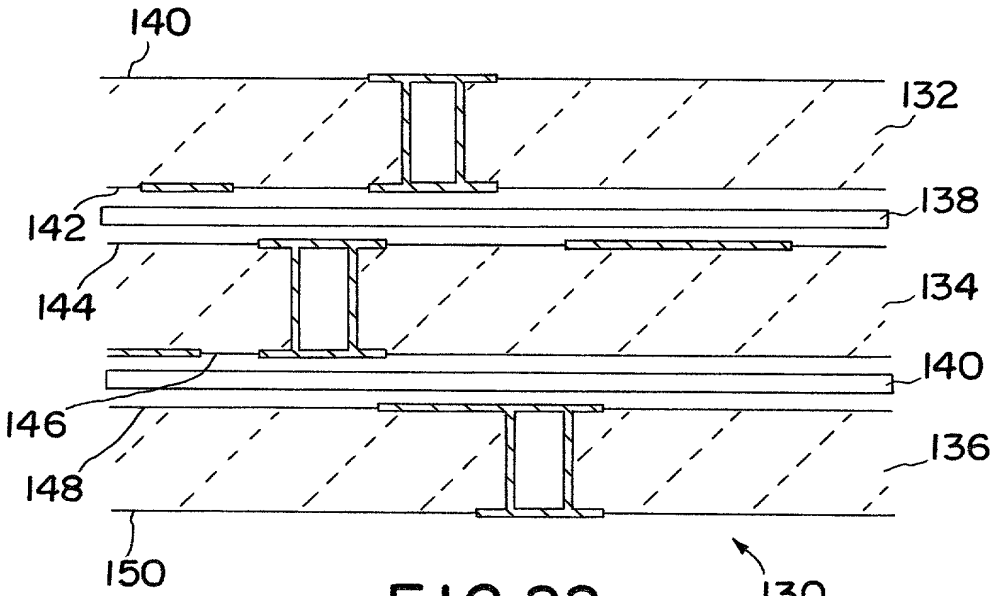

FIG. 22

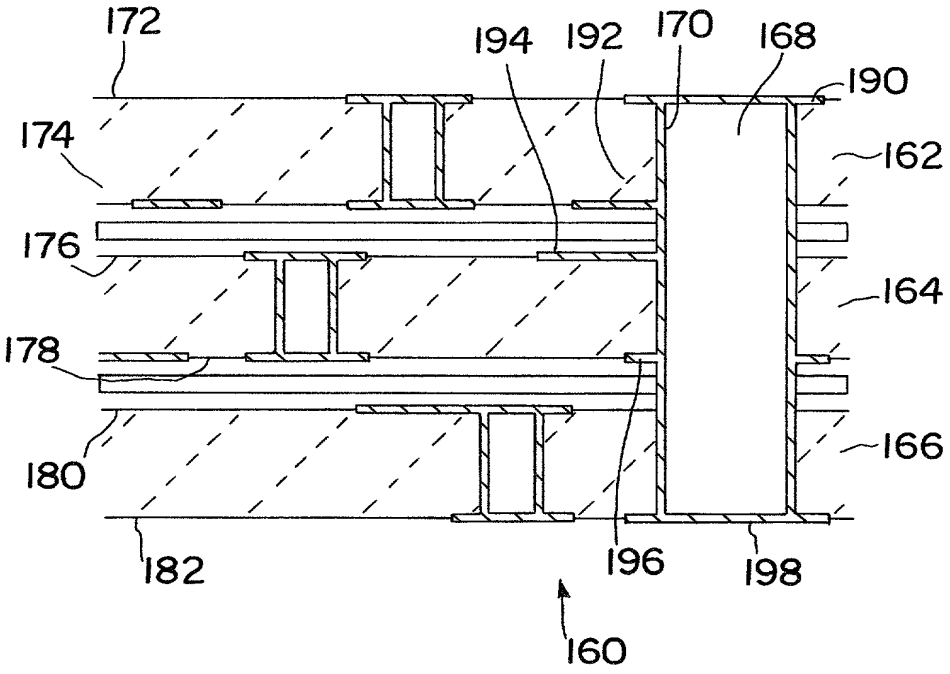
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FIG. 23

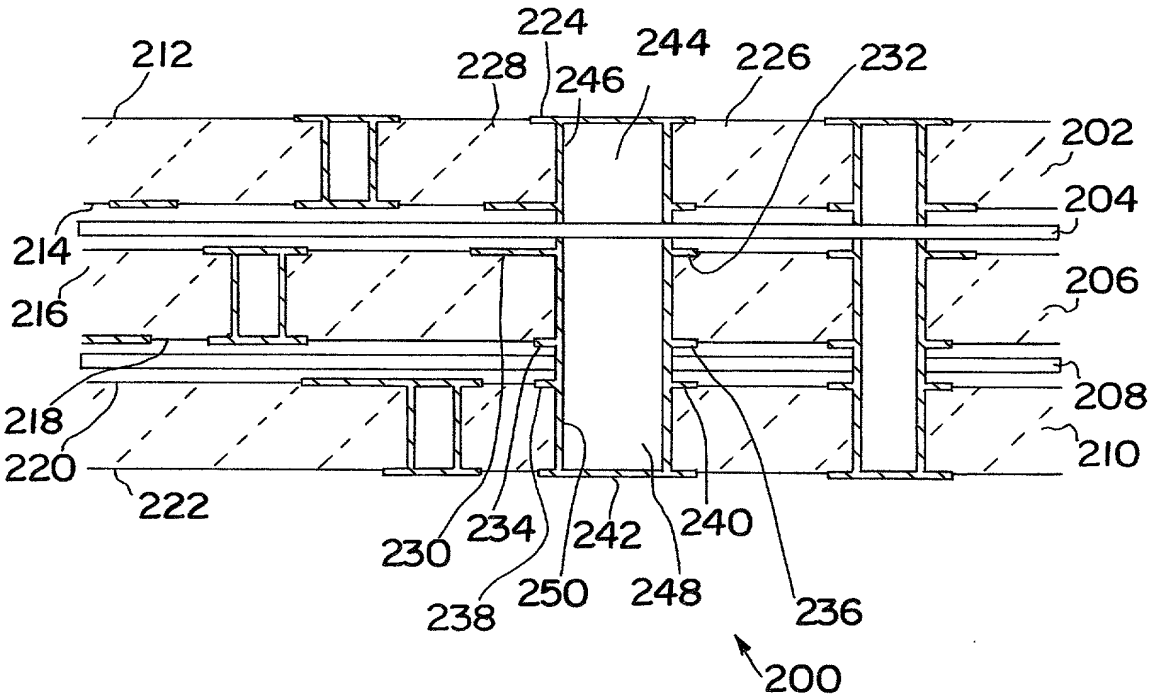
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FIG. 24

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No: BERG 99.01 CIP

First Named Inventor: BERG

Complete if known: Serial No: _____ Filing Date: August 1, 2001

Group Art Unit: _____ Examiner: _____

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **Improved Circuit Board Manufacturing Process**, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, S. 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	Certified Copy Attached
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes ☐ No	☐ Yes ☐ No
(Number)	(Country)	(Month/Day/Year Filed)	☐ Yes ☐ No	☐ Yes ☐ No

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below:

Application No:	Filing Date:
60/118,263	February 2, 1999
60/152,532	September 3, 1999

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

US Parent Application No. or PCT Parent Appln. No.	Parent Filing Date	Parent Patent Number (if applicable)
PCT/US00/02543	February 1, 2000	

And I hereby appoint HAYES, SOLOWAY, HENNESSEY, GROSSMAN & HAGE, P.C., a firm composed of Oliver W. Hayes, Reg. No. 15,867; Norman P. Soloway, Reg. No. ~~24,315;~~ William O. Hennessey, Reg. No. ~~32,032;~~ Susan H. Hage, Reg. No. 29,646; ~~S~~teven J. Grossman, Reg. No. ~~35,001,~~ and Donald J. Perreault, Reg. No. ~~40,126,~~ or any of them, of 175 Canal Street, Manchester, New Hampshire 03101 (Telephone: 603-668-1400); or Edmund Paul Pfleger, Reg. No. ~~41,252;~~ Dale F. Regelman, Reg. No. 45,625; or Kevin M. Drucker, Reg. No. ~~47,537,~~ or any of them, of 130 W. Cushing Street, Tucson, Arizona 85701 (Telephone: 520-882-7623) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith.

Please direct all future correspondence in connection with this application to the attention of **Norman P. Soloway,** HAYES, ~~SOLOWAY, HENNESSEY,~~ GROSSMAN & HAGE, P.C., 130 W. Cushing Street, Tucson, ~~Arizona 85701 (Tele~~phone: 520-882-7623).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: **N. Edward Berg**

First Inventor's signature N Edward Berg Date 23 July 2001
Residence: 70 Horizon Drive, Bedford, New Hampshire 03110
Citizenship: USA
Post Office Address: Same as Residence

IMPORTANT NOTICE RE DUTY OF CANDOR AND GOOD FAITH

The Duty of Disclosure requirements of Section 1.56(a), of Title 37 of the Code of Federal Regulations are as follows:

A duty of candor and good faith toward the Patent and Trademark Office rests on the inventor, on each attorney or agent who prepares or prosecutes the application and on every other individual who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application. All such individuals have a duty to disclose to the Office information they are aware of which is material to the examination of the application. Such information is material where there is a substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent. The duty is commensurate with the degree of involvement in the preparation or prosecution of the application.

By virtue of this regulation each inventor executing the Declaration for the filing of a Patent Application acknowledges his duty to disclose information of which he is aware and which may be material to the examination of the application.

Inherent in this is the duty to disclose any knowledge or belief that the invention:

(a) was ever known or used in the United States of America before his invention thereof;

(b) was patented or described in any printed publication in any country before his invention thereof or more than one year prior to the actual filing date of the U.S. patent application;

(c) was in public use or on sale in the United States of America more than one year prior to the actual filing date of the U.S. patent application; or

(d) has been patented or made the subject of inventor's certificate issued before the actual filing date of the U.S. patent application in any country foreign to the United States of America on an application filed by him or his legal representatives or assigns more than twelve months before the actual filing date in the United States.

NOTE: The "Information" concerned includes, but is not limited to, all published applications and patents, including applicant's and assignee's own, U.S. or foreign applications and patents, as well as any other pertinent prior art known, or which becomes known, to the inventor or his representatives. Where English language equivalents of foreign language documents are known, they should be identified and, when possible, copies supplied. Failure to comply with this requirement may result in a patent issued on the application being held invalid even if the known prior art which is not supplied is material to only one claim of that patent.